ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

High Voltage Circuits Implemented Using Low Voltage Transistors

Application Number: 10/710,692

Confirmation Number:

First Named Applicant:

Sanish JACOB

Attorney Docket Number:

TI-37611

Art Unit:

2815

Examiner:

SHINGLETON

Search string:

(4704547).pn

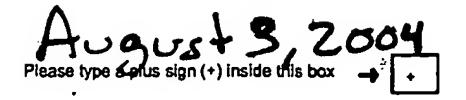
US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
MS	1	4704547	1987-11-03	Kirsch			

Signature

Examiner Name	Date
SHINGLETON	2/28/2007



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PTO/SB/08A (08-00)

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				U.S. PATENT DOCUM	ENTS	
	Cite	U.S. Patent Document Number		Name of Patentee or Applicant	Date of Publication of cited Document	Pages, Columns, Lines, Where Relevant
	No. ¹			of Cited Document	MM-DD-YYYY	Passages or Relevant Figures Appear
MS		4,704,547		Kirsch; Howard C.	11-03-1987	3
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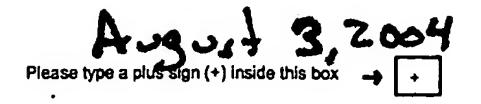
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^{*}EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). * For Japanese patent documents, the Indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as Indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.



two sheets

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number. Substitute for form 1449B/PTO Complete if Known 10/710,692 **Application Number** INFORMATION DISCLOSURE **Filing Date** July 28, 2004 STATEMENT BY APPLICANT **First Named Inventor** Sanish koshy jacob **UNASSIGNED Group Art Unit** (use as many sheets as necessary) ULILETON **UNASSIGNED Examiner Name Attorney Docket Number** 2 of 2 TI-37611 Sheet

		OTHER PRIOR ART - NON PATENT LITER	ATURE DOCU	MENTS			
Examin er Initials*	Cite No. ¹						
MBI		Hector Sanchez, Joshua Siegel, Carmine Nicoletta, James .p V CMOS I/O Driver Bulit in a 0.2-um ,3.5-nm Tox, 1.8-V Cl Circuits Vol 34. pp. 1501-1511, No.11, November 1999.					
mbs		Changsik Yoo, Min -Kyu Kim , and Wonchan kim , " A Static F Journal of Solid State Circuits. Vol 30, pp. 616- 620, No. 5,		L-to -CMOS Input buffer in IEEE			
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Examiner SHINGLETON Date Considered 2-28-07

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